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April 30, 2004

Commissioner for Patents P.O.Box 1450 Alexandria, VA 22313-1450

Fr: George O. Saile, Reg. No. 19,572 28 Davis Avenue Poughkeepsie, N.Y. 12603

Subject:

Serial No. 10/789,083 02/27/04

Bang-Ching Ho et al.

METHOD OF FORMING A DUAL DAMASCENE STRUCTURE

INFORMATION DISCLOSURE STATEMENT

Enclosed is Form PTO-1449, Information Disclosure Citation
In An Application.

The following Patents and/or Publications are submitted to comply with the duty of disclosure under CFR 1.97-1.99 and 37 CFR 1.56.

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on May $\mathcal G$, 2004.

Stephen B. Ackerman, Reg.# 37761

Signature/Date

- U.S. Patent 6,365,529 to Hussein et al., "Method for Patterning Dual Damascene Interconnects Using a Sacrificial Light Absorbing Material," reveals a method for forming dual damascene copper interconnects using a reactive ion etching of a sacrificial layer that fills the previously formed contact hole.
- U.S. Patent 6,350,681 to Chen et al., "Method of Forming Dual Damascene Structure," reveals a dual damascene process that uses a chemical mechanical polishing process to remove the barrier layer material outside the via holes.
- U.S. Patent 6,268,283 to Huang, "Method for Forming Dual Damascene Structure," discloses a transparent spun on cap layer underneath the resist to prevent damage by the developer to the dielectric underlayers.
- U.S. Patent 6,013,581 to Wu et al., "Method for Preventing Poisoned Vias and Trenches," discloses a dual damascene process that includes a plasma treatment of the exposed dielectric layer below the opening before the openings are filled with conductive material.

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U.S. Patent 6,057,239 to Wang et al., "Dual Damascene Process Using Sacrificial Spin-On Materials," discloses a dual damascene process that exposes a portion of the oxide layer by using reactive ion etchback of the antireflective layer that filled the contact hole.

Some papers have been published that reflect on the issues of conventional dual damascene and these include using a BARC (bottom antireflective layer) layer such as in Ding et al., "Optimization of Bottom Antireflective Coating Materials for Dual Damascene Process," SPIE Proceedings, 3999,910-918(1999), Pollentier et al., "Dual Damascene back-end Patterning using 248 nm and 193 nm Lithography," Interface 2000, pps. 265-284(2000), and Gadson, Solid State Technology, pp. 77(2001).

Sincerely

Stephen B. Ackerman,

Reg. No. 37761

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